A 1.6 GHz 0.5 mW CMOS LC Low Phase Noise VCO Using Bond Wire Inductance

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Areas: RF circuits, low-voltage low-power circuits

ABSTRACT

A 1.6-GHz LC voltage-controlled oscillator has been implemented in a 0.5-µm CMOS process. Bond wires, with their low series resistance, provide a resonant tank with high Q. Complementary cross-coupled PMOS and NMOS transistors enhance the single-ended symmetry at each of the resonant nodes to reduce close-in phase noise. At an offset frequency of 100 kHz, the measured phase noise is -95 dBc/Hz at a 0.5 mW power dissipation from a 2.0 V supply. An 8.7% tuning range is achieved using NMOS gate capacitors.

Introduction

The popularity of personal communication systems in the GHz range urges circuit designers towards more compact and more cost-effective solutions. The current target is a monolithic RF receiver, where one of the largest hurdles remaining is a fully integrated, low noise, low power voltage-controlled oscillator (VCO). For higher quality receivers, an LC oscillator topology is typically chosen over a relaxation oscillator or a ring oscillator topology because the bandpass nature of the resonant tank in the LC oscillator renders the lowest phase noise for a given amount of power.

Still, the inability to manufacture or synthesize a high quality on-chip inductor has inhibited the complete integration of an LC oscillator. Bond wires, however, with their low series resistance, hold significant promise over spiral inductors [1] and active inductors [2] for tendering a high Q, low phase noise solution.

In this paper, we present an LC voltage-controlled oscillator fabricated through MOSIS in a 0.5-µm CMOS process using bond wires to implement the inductors.

LC VCO Design

The primary trade-off in the design of an integrated oscillator is between low phase noise and power dissipation. In the past, designers have typically presumed that the $1/f^3$ phase noise corner coincides with the $1/f$ device noise corner. The Hajimiri phase noise model [3] reveals that the $1/f^3$ phase noise corner is affected by the waveform symmetry of the oscillator, and differs from the device $1/f$ corner as formerly assumed. The trade-off between low phase noise and power dissipation still exists in the $1/f^2$ region, but there is room for improvement in the $1/f^3$ region by exploiting properties of symmetry. This improvement is of greater importance for CMOS oscillators, since CMOS transistors exhibit a higher $1/f$ noise corner.

Therefore, there are now two considerations when trying to minimize phase noise. The first was demonstrated by Craninckx and Steyaert [4]. Their work focuses on increasing signal energy by using a tapped resonant tank. They ignore the effects of asymmetry on the circuit. The second concern, and the one explored in this paper, is single-ended waveform symmetry. Any asymmetry in the waveform allows low frequency noise to be upconverted and increase the $1/f^3$ corner of the phase noise. Noise sources in each half circuit are uncorrelated with the noise sources in the other half circuit; thus, the noise cannot be treated simply as a common-mode signal. In this paper, we focus solely on the effects of symmetry and ignore any gains from tapping the resonant tank.

To achieve this symmetry and to test its viability for reducing phase noise, we chose the negative-resistance topology shown in Figure 1. The goal of this design was a 1.6-GHz LC VCO with minimum phase noise on 0.25 mA with a 2.0 V supply.

The cross-coupled NMOS transistors, M1 and M2, provide the negative resistance to cancel the losses presented by the parallel LC tank at resonance. The cross-coupled PMOS transistors, M3 and M4, are twice the width of their NMOS counterparts and increase the loop gain. More important, the PMOS devices allow better symmetry to be achieved on each of the resonant nodes by equating the positive and negative drive strength. It is this topology, with attention to symmetry on both the full circuit and each half circuit, that reduces phase nose.

The varactor is implemented by standard NMOS gate capacitors operated near threshold. There are two capacitors, each with the source/drain connection to the resonant nodes. Using two capacitors easily preserves symmetry, while the shared gate node is driven by the control voltage. The losses in this type of capacitor are large, though, leading to a low Q value. Therefore, its magnitude was chosen to be a small percentage of the

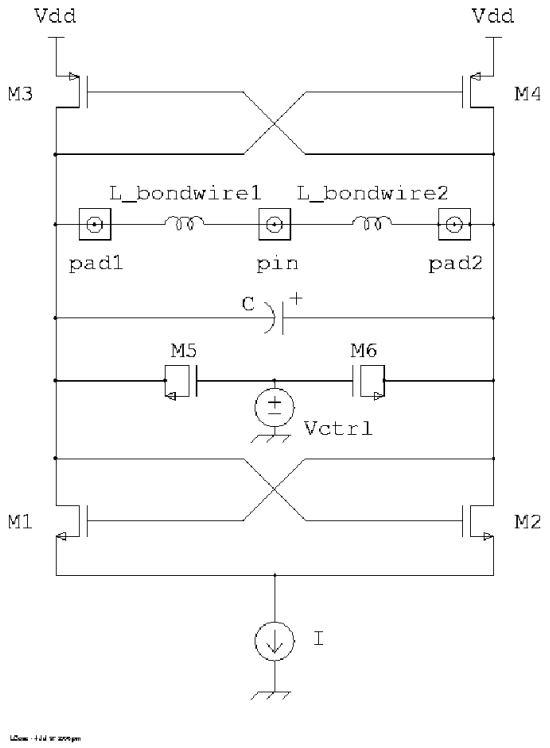

Figure 1: Circuit Diagram

total effective tank capacitance, while remaining large enough to provide adequate tuning range.

Two bond wires comprise the tank inductance. One traverses from the bond pad on the die to the package, and the other follows the return path. This method maintains the symmetric architecture between the differential output nodes. About 4 nH of inductance is supplied by 4 mm of bond wires. The extra capacitance of the package at the center of the two inductors is unimportant since this node is a differential-mode ground.

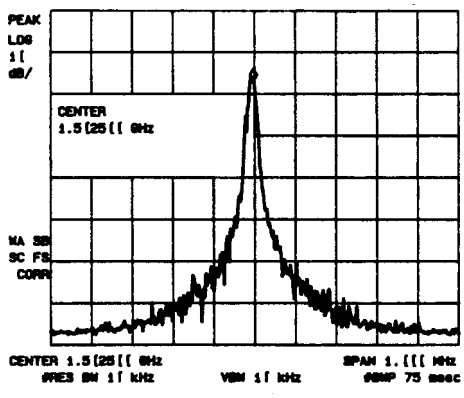

Figure 2: Output spectrum of oscillator

The total inductance of the tank structure is estimated at approximately 6 nH. Some additional inductance was necessary to increase the loop gain and initiate oscillation at the expense of lowering the center frequency of the oscillator. This additional 2nH was added as a board trace between two pins, once the die was rebonded so that the bondwire inductors connected to adjacent pins on the package instead of the same pin.

Experimental Results

After some additional inductance was added to the resonant tank through a board trace, the output was coupled to the spectrum analyzer through a coil of wire acting as an antenna. This output is shown in Figure 2.

The varactor provides the flexibility to achieve oscillation frequencies from 1.47 GHz to 1.60 GHz, representing an 8.7% tuning range. Figure 3 reveals the VCO's frequency versus voltage characteristic.

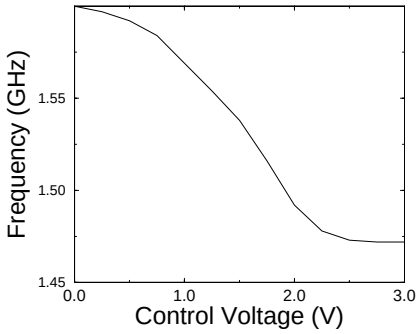

Figure 3: Output frequency versus control voltage

The phase noise, measured on an HP 8590B spectrum analyzer, is -95 dBc/Hz at 100 kHz for the 1.6-GHz signal. The experiment was repeated at a smaller offset frequency where the close-in phase noise would be easier to measure. At an offset of 10 kHz, the measured phase noise is -64dBc/Hz.

For comparison, the phase noise is also measured at a supply voltage of 3.3 volts. With 0.25 mA of bias current, the phase noise measured -98 dBc/Hz at an offset frequency of 100 kHz and -68 dBc/Hz at an offset frequency of 10 kHz.

For currents greater than 0.30 mA, the phase noise actually increases because the oscillator swing becomes voltage limited. When the oscillator swing is voltage limited, the PMOS and NMOS transistors no longer remain in the saturation region for the entire oscillation cycle. For the period of time that they enter the linear region, they no longer present a negative resistance to the LC tank. This cyclostationary effect degrades the phase noise.

Previous work [4] [5] with bond wire LC oscillators has shown that bond wires could be utilized to manufacture a high quality solution to the integrated

receiver challenge. To date, the most promising results [4] display a phase noise measurement of -115 dBc/Hz for a 200 kHz delta frequency on 24 mW at 1.8 GHz. In comparison, this paper presents a configuration displaying a phase noise of approximately -95 dBc/Hz for an 100 kHz offset frequency on 0.5 mW at 1.6 GHz. This result also compares quite favorably with a recent 1.6 GHz bipolar implementation which achieved -95.1 dBc/Hz at a 100 kHz offset with 3mW and an external resonator [7].

A summary of the experimental results is provided in Table 1.

Table 1: Summary of Results

Center Oscillation Frequency	1.6 GHz
Supply Voltage	2.0 volts
Power Consumption	0.5 mW
Tuning Range	130 MHz
Phase Noise @ 10 kHz	-64 dBc/Hz
Phase Noise @ 100 kHz	-95 dBc/Hz
Process Technology	0.5-µm standard CMOS

Conclusion

We have demonstrated the viability and performance of bond wire inductors in a 1.6 GHz LC VCO fabricated in a standard 0.5-µm CMOS process. The design yields -95 dBc/Hz phase noise at an offset frequency of 100 kHz on a mere 0.5 mW. This achievement is a result of lowering the $^1/_{f^3}$ corner by enforcing a previously unappreciated symmetry constraint on each of the two differential output nodes of the oscillator.

Acknowledgments

The authors would like to acknowledge Rafael Betancourt-Zamora for his constant encouragement and assistance in making this project possible.

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