Brief Papers

A 0.8-dB NF ESD-Protected 9-mW CMOS LNA Operating at 1.23 GHz

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***Abstract*—In recent years, much research has been carried out on the possibility of using pure CMOS, rather than bipolar or BiCMOS technologies, for radio-frequency (RF) applications. An example of such an application is the Global Positioning System (GPS). One of the important bottlenecks to make the transition to pure CMOS is the immunity of the circuits against electrostatic discharge (ESD). This paper shows that it is possible to design a low-noise amplifier (LNA) with very good RF performance and sufficient ESD immunity by carefully co-designing both the LNA and ESD protection. This is demonstrated with a 0.8-dB noise figure LNA [1] with an ESD protection of −1.4–0.6 kV human body model (HBM) with a power consumption of 9 mW. The circuit was designed as a standalone LNA for a 1.2276-GHz GPS receiver. It is implemented in a standard 0.25-μm 4M1P CMOS process.**

***Index Terms*—CMOS integration, ESD protection, GPS, low-noise amplifier, receiver front ends, RF, wireless.**

I. Introduction

THE PERFORMANCE requirements of high-end GPS receivers are quite tough, requiring a receiver with good sensitivity performance as well as a low-noise amplifier (LNA), characterized by an excellent noise figure. To cope with these requirements, high-performance GaAs MESFET LNAs are often used, because they are capable of offering excellent noise figures in the order of 1 dB at large power gains of 20 dB. Using a GPS LNA as a test vehicle, this work will prove that even in a standard submicron CMOS technology, an extremely low noise figure (<1 dB) and a high gain (20 dB) can be achieved at the same power consumption as commercially available GaAs LNA solutions.

The 0.25-μm CMOS LNA described in this work [1] offers a noise figure as low as 0.8 dB at a power gain of 20 dB while consuming only 9 mW, outperforming previously published CMOS LNAs with respect to noise figure, gain, and power consumption. In addition, the IC contains an electrostatic discharge (ESD) protection on the radio-frequency (RF) input pad which is capable of protecting the LNA against −1.4–0.6 kV human body model (HBM) pulses. This demonstrates that an excellent performance can be achieved while at the same time providing $>$ 0.5 kV ESD protection.

Section II reviews the power levels of the GPS application and the typical requirements for a GPS LNA. The actual design tradeoffs of the realized LNA are presented in Section III. The experimental results are discussed in Section IV.

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TABLE I
MINIMUM GPS RECEIVE POWER LEVELS

	P code	C/A code
L1	-133 dBm	-130 dBm
L2	-136 dBm	-136 dBm

II. GPS Power Levels and LNA Requirements

Table I shows the minimum specified received signal strength for the different GPS signals. For civil GPS, the second column (the C/A code) is the relevant one. In the L1 band (broadcast at 1.575 GHz), the minimum received power is −130 dBm. This gives us an effective signal-to-noise ratio (SNR) of about 29 dB at the input of the receiver. In the L2 band (broadcast at 1.2276 GHz), the minimum received power is even 6 dB lower, yielding an effective SNR of 23 dB. In practice, the SNR of the received signal is much worse. In urban canyons or when tree foliage shadows the user, the minimum received power often is much lower than the specified −130 dBm. The SNR can be degraded by as much as 10–20 dB.

Therefore, to keep the receiver from giving up early, the receiver noise figure must be very low, which poses severe demands on both the noise figure and the gain of the RF input amplifier. In order to prove the suitability of CMOS for building extremely sensitive receivers, one must demonstrate the feasibility of achieving very low noise figures ($\leq$ 1 dB) and large gains (18–20 dB) at a power consumption comparable to GaAs solutions. In [1], a CMOS LNA was presented which consumes less than 10 mW while offering a performance comparable to commercial GaAs LNAs.

III. Design

A. Topology

The LNA has been implemented as an inductively degenerated common source amplifier (Fig. 1), which amplifies the antenna power while presenting a 50-Ω input impedance to the antenna. Cascode transistor M_2 drastically reduces the Miller effect by ensuring a low impedance at the drain of the amplifying device. This keeps the Miller effect from degrading the power gain, as well as from increasing the input referred noise. In addition, the cascode improves the reverse isolation,

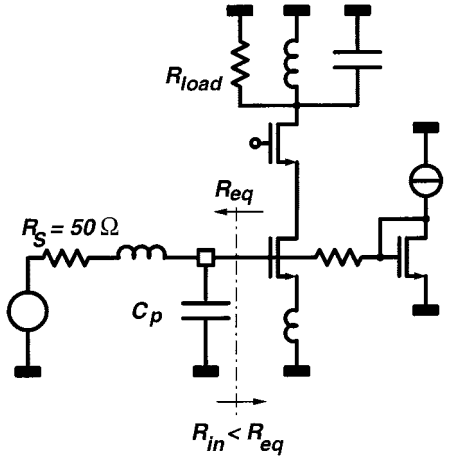

Fig. 1. Input matched common source, cascode LNA.

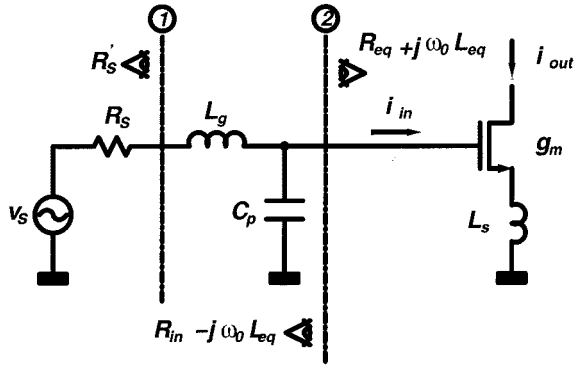

Fig. 2. Input section of the LNA.

increases the stability, and causes the output matching network and the input matching network to no longer influence each other. The input of the LNA is protected against ESD by two reverse-biased diodes. The output is matched to 50 Ω by a capacitive divider made up of C_1 and C_2.

B. Theory

The input of the LNA is shown in Fig. 2. A certain amount of parasitic capacitance $C_{\rm p}$ is always present. Part of it comes from the input bonding pad; another part could stem from an ESD-protection network at the input. It is instructive to define two reference planes 1 and 2 and to look at the different impedance levels at these nodes. $R_{\rm S}$ denotes the impedance of the source which is the output impedance of the previous building block, either an antenna or a channel-select filter. In this case, $R_{\rm S}$ is simply 50 Ω. $R'_{\rm S}$ denotes the input impedance of the LNA seen at reference plane 1. The equivalent source impedance seen to the left of reference plane 2 is given by $R_{\rm eq} + j\omega L_{\rm eq}$, where $R_{\rm eq}$ and $L_{\rm eq}$ are given by

$$R_{\rm eq} = \frac{R_{\rm S}}{\omega_0^2 C_{\rm p}^2 R_{\rm S}^2 + \left(1 - \omega_0^2 C_{\rm p} L_g\right)^2} \tag{1}$$

$$L_{\rm eq} = \frac{L_g - C_{\rm p}\left(\omega_0^2 L_g^2 + R_{\rm S}^2\right)}{\omega_0^2 C_{\rm p}^2 R_{\rm S}^2 + \left(1 - \omega_0^2 C_{\rm p} L_g\right)^2}. \tag{2}$$

Finally, $R_{\rm in} - j\omega L_{\rm eq}$ denotes the input impedance of the LNA seen at reference plane 2.

Traditionally, the value of $R'_{\rm S}$ would be designed to equal $R_{\rm S}$, i.e., 50 Ω. However, since the required S_{11} is typically only −10 dB, an extra degree of freedom can be introduced by realizing a nonperfect input match. This can be used to boost the performance of the LNA and, more specifically, the power gain of the circuit. The available power of the source is by definition given by

$$P_{\rm av} = \frac{v_{\rm eq}^2}{4R_{\rm eq}} = \frac{v_s^2}{4R_{\rm S}} \tag{3}$$

where $R_{\rm S} = 50\,\Omega$. The output power of the LNA is determined by the equivalent load resistance $R_{\rm load}$ of the LNA and by the current injected in that load:

$$P_{\rm out} = i_{\rm out}^2 R_{\rm load}. \tag{4}$$

$R_{\rm load}$ mainly consists of the equivalent parallel resistance of the load inductor.

$$R_{\rm load} \approx \frac{\omega_0^2 L_d^2}{R_{\rm s}} \tag{5}$$

where $R_{\rm s}$ is the series resistance of the inductor L_d. The inductance itself is tuned out by the excess capacitance at that node. The output current $i_{\rm out}^2$ is given by

$$i_{\rm out}^2 = i_{\rm in}^2 \left(\frac{\omega_T}{\omega_0}\right)^2 \tag{6}$$

where

$$i_{\rm in}^2 = \frac{4P_{\rm av}R_{\rm eq}}{\left(R_{\rm eq} + R_{\rm in}\right)^2}. \tag{7}$$

From (3), (4), (6), and (7), the power gain of the LNA may be calculated, as follows:

$$G_t = \frac{R_{\rm eq}R_{\rm load}}{\left(R_{\rm eq} + R_{\rm in}\right)^2}\left(\frac{\omega_T}{\omega_0}\right)^2. \tag{8}$$

It is seen that the highest level of power gain for a given frequency and value of ω_T is obtained by making the input impedance $R_{\rm in}$ as low as possible. This means that even though less power is absorbed at the input of the LNA, the power is used more efficiently to generate output current and, hence, output power. Note that for input matching, it is important to include the non-quasi-static (NQS) effect, a phase lag in the channel charge buildup. Although it is an inherently high-frequency (≈ 100 GHz) effect, due to the resonance at the LNA input, the NQS is seen as an extra gate resistance [6].

$$R_{\rm g,NQS} = \frac{1}{\kappa g_m} \quad \kappa = 5. \tag{9}$$

This implies that $R_{\rm in}$ can never be set lower than $R_{\rm g,NQS}$ (around 20 Ω).

Noise considerations are also best done on the reference plane of $R_{\rm eq}$ (see Fig. 2). The non-quasi-static effect should be taken into account in the noise analysis. It implies a time-variant channel charge, resulting in an equivalent input noise current,

yielding the following approximate expression for the noise figure (NF) of the LNA [6]:

$$\mathrm{NF} \simeq 1 + \underbrace{\left(\frac{\omega_0}{\omega_T}\right)^2 \frac{\gamma}{\alpha} g_m R_{\mathrm{eq}}}_{\text{Classic Noise}} + \underbrace{\left(\frac{\omega_0}{\omega_T}\right)^2 \frac{\gamma}{\alpha}\frac{2}{\kappa} + \frac{\alpha\delta}{\kappa g_m R_{\mathrm{eq}}}}_{\text{NQS Noise}} \tag{10}$$

with α, γ, and δ known transistor parameters. In case of high R_{eq}, the noise is determined by the classic drain noise, but at low R_{eq}, the NF increases again due to the NQS noise. Equation (1) has shown that a larger parasitic capacitance C_{p} will increase the equivalent source resistance R_{eq}. Since C_{p} is almost always high enough for the classic noise to dominate, the insertion of the ESD protection will significantly degrade the noise figure. Based on (3)–(10), it is further seen that the NF decreases and the power gain increases with increasing ω_T. As such, deeper submicron technologies automatically improve both the NF and gain of the LNA.

The dependence of the LNA linearity, characterized by its input-referred third-order intercept point (IIP3), on the $V_{\mathrm{GS}} - V_{\mathrm{T}}(V_{\mathrm{gt}})$, technology and input matching is shown in (11).

$$\mathrm{IIP3} \simeq 10\log\left(\frac{4}{3}\frac{V_{\mathrm{gt}}\left(1+\Theta V_{\mathrm{gt}}\right)^2\left(2+\Theta V_{\mathrm{gt}}\right)}{\Theta}\right) + 20\log\left(\omega_0 C_{\mathrm{gs}}\left(R_{\mathrm{eq}}+R_{\mathrm{in}}\right)\sqrt{\frac{50\,\Omega}{R_{\mathrm{eq}}}}\right) - 10. \tag{11}$$

For a transistor without matching section [first term of (11)], the IIP3 improves with increasing $V_{\mathrm{GS}} - V_{\mathrm{T}}$ and deteriorates with deeper submicron technologies. Although the MOS seems to "linearize" for decreasing gate lengths due to velocity saturation (given by Θ), the effect on intermodulation gets worse for $V_{\mathrm{GS}} - V_{\mathrm{T}} \lesssim 0.25$ V. For a matched transistor, the dependencies become more complex because the IIP3 decreases with decreasing equivalent source resistance R_{eq}. This is shown in the second term. The final term converts the units from $\mathrm{dBV_{amp}}$ to dBm.

Since the value of R_{eq} is determined by the amount of parastic capacitance C_{p} (1), a tradeoff exists between the linearity, gain, and noise performance and the required level of ESD protection. After this value is set, the performance of the LNA may be optimized by considering the power consumption versus $V_{\mathrm{GS}} - V_{\mathrm{T}}$ using (3)–(11) to realize the specifications.

C. Optimization

A basic schematic of the LNA is shown in Fig. 3. In order to clarify the design tradeoffs, Figs. 4–6 show contour plots (based on the previous equations) of the most important LNA properties in the design space of the amplifying device. In these plots, it is assumed that the input capacitance C_{p} is set to 210 fF, i.e., 110 fF for the bondpad and 100 fF for the protection diodes. This capacitance ensures a level of ESD protection exceeding the 0.5-kV HBM protection level that was specified.

Fig. 4 depicts the NF of the LNA under ideal circumstances (i.e., assuming a lossless L_g, L_s, etc.). As can be seen from the plot, the noise figure is extremely low in the whole design space. The LNA does not even need the available 6 mA; according to the plot, a noise figure as low as 0.3 dB can already be achieved at a drain current of only 1.1 mA. Fig. 5 plots the contour lines of the IIP3 of the LNA. Clearly, 6 mA is not even required from a linearity perspective; an IIP3 of -6 dBm can already be obtained at about 3 mA. However, 6 mA is needed in order to obtain sufficient power gain, as is explained below.

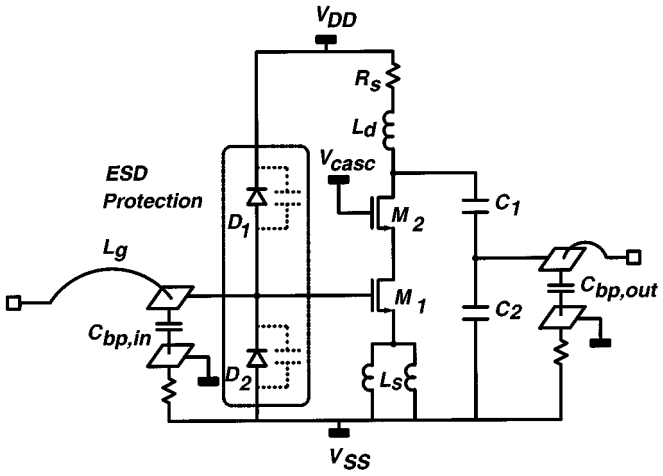

Fig. 3. The 50-Ω cascode LNA circuit.

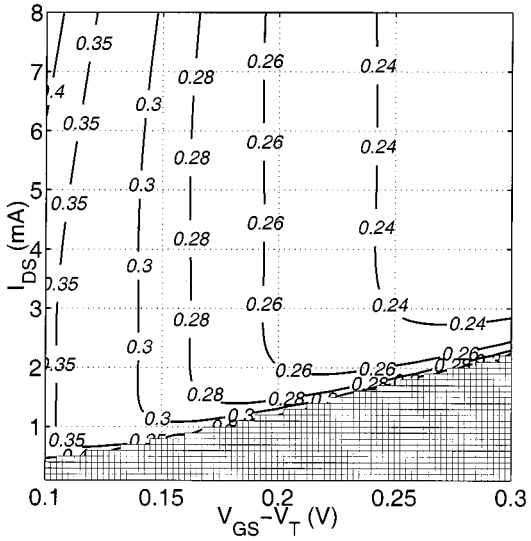

Fig. 4. Contour plots of the total LNA noise figure (dB).

Fig. 6 indicates that the required effective R_{load} at the drain of the cascode becomes large when biasing the input stage at low current levels. This can be attributed to the drop in the efficiency of the amplifying device due to the increase in the equivalent source impedance R_{eq} seen by the input transistor. The fact that inductors with a large R_{load} do indeed pose some problems can be explained by the following reasoning. Any practical system must be able to tolerate process variations. One of the requirements could be that the operating frequency must lie in the -3 dB bandwidth of the amplifier despite a $\pm\Delta\omega_0$ deviation in the center frequency. This requirement translates into the following constraint on the total LNA quality factor Q:

$$Q_{\mathrm{LNA}} \leq \frac{\omega_0}{2\Delta\omega_0}. \tag{12}$$

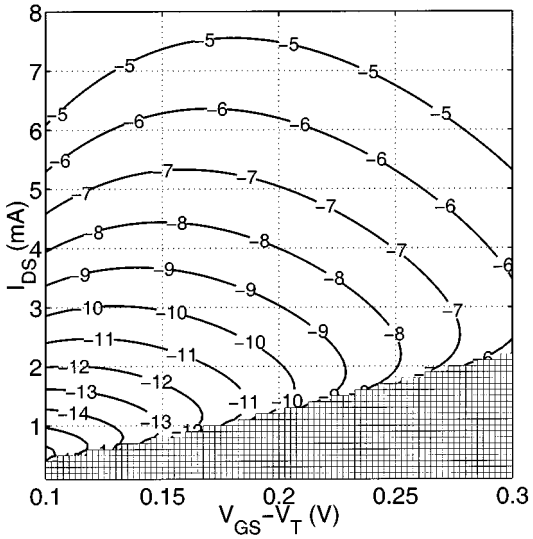

Fig. 5. Contour plots of the IIP3 (dBm).

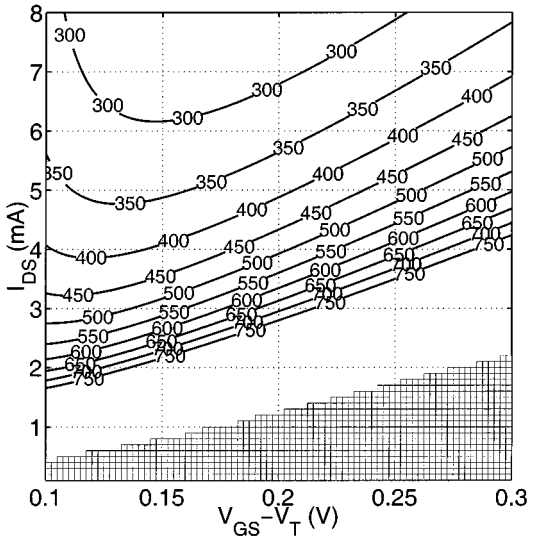

Fig. 6. Contour plots of the required inductor $R_{\rm load}$ $[\Omega]$.

For instance, in the case that $\Delta\omega_0 = \pm 0.1\omega_0$, $Q_{\rm LNA}$ must be smaller than 5. The $Q_{\rm LNA}$ value consists of two contributions: the quality factor of the input (generally close to one because of the bondpad/protection capacitance) and the quality factor of the output section, which is mainly determined by the inductor. Stating $R_{\rm load}$ in terms of the quality factor of the inductor yields

$$R_{\rm load} = \left(Q_L + \frac{1}{Q_L}\right)\omega_0 L_d \cong Q_L \omega_0 L_d. \qquad (13)$$

Since Q_L needs to be smaller than the value calculated in (12) (diminished by the quality factor of the input section), an inductor with a large $R_{\rm load}$ must necessarily exhibit a relatively large inductance value. Yet, considering that the resonance frequency must remain the same, this strongly limits C_1 and C_2, which makes the matching network very sensitive to external parasitics.

In view of the above, the $I_{\rm DS}$ and the $V_{\rm GS} - V_{\rm T}$ of the amplifying device have been set to 6 mA and 0.14 V, respectively.

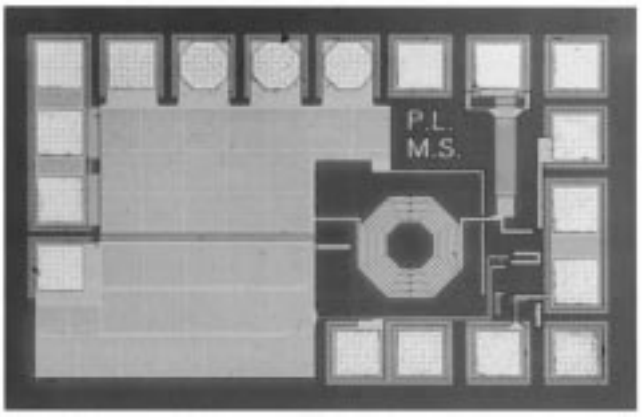

Fig. 7. LNA micrograph.

At this point, the quality factor of the input section equals 0.9, leaving a maximum of 4.1 for Q_L. On the other hand, Fig. 6 indicates that the effective $R_{\rm load}$ must be around 310 Ω. This resulted in a 10.5-nH inductor with a 20-Ω series resistance, equivalent with a Q_L of 4 and an $R_{\rm load}$ of about 330 Ω.

Since the LNA was designed as a standalone circuit with both input and output impedance equal to 50 Ω, achieving a maximum power transfer requires that the 50-Ω load is transformed into the complex conjugate of the effective output impedance at the drain of the cascode. In other words, the matching network must transform the 50-Ω load into a resistive path with impedance $R_{\rm load}$ and at the same time generate the exact amount of parallel capacitance to cancel out the effective inductance at the drain of the cascode. Therefore, the rest of the matching network must contain two degrees of freedom. In this particular circuit, these degrees of freedom are offered by the quasi-lossless capacitive divider C_1/C_2 [5]. In fact, for each realizable inductor, there exists a realizable combination of C_1 and C_2 values that provides the correct impedance, provided that:

1) the inductor is not self-resonant at frequencies near or below the operating frequency;
2) the required capacitance from the output node to $V_{\rm SS}$ is larger than the minimum possible, which is limited by the sum of the parasitic capacitance of the output bondpad and the stray capacitance of C_1 toward the substrate.

IV. Experimental Results

A photograph of the IC is shown in Fig. 7. The IC is implemented in a standard 0.25-μm 4M1P CMOS process and occupies an area of 0.66 mm^2. To measure the LNA, the IC is glued onto a thick film ceramic substrate, and all the pads are wire bonded to 50-Ω microstrip lines. The gate inductor is implemented as a bondwire because of its low series resistance and its low parasitic capacitance. The substrate is then mounted in a copper–beryllium box which shields the LNA from external interference and serves as reference ground. The connection to the external world is provided through two SMA connectors. The LNA is biased in its nominal 9-mW regime, i.e., drawing 6 mA from a 1.5-V supply. First, the complete S-parameter set has been measured using an HP network analyzer. The forward gain

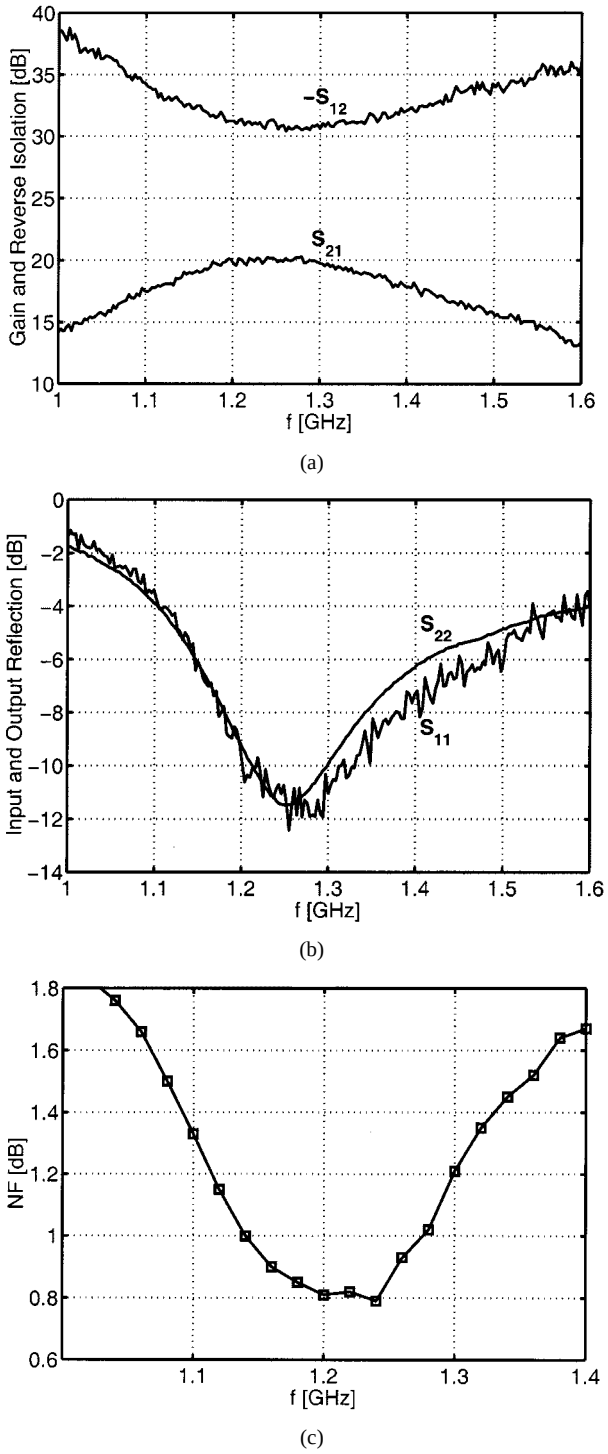

Fig. 8. Measured LNA performance. (a) Gain and reverse isolation. (b) Input and output reflection. (c) Noise figure.

(transducer power gain, S_{21}), plotted in Fig. 8(a), is measured to be a flat 20 dB in a 100-MHz-wide band around the GPS L2 frequency of 1.2276 GHz (1.2–1.3 GHz). The -3 dB bandwidth is approximately 400 MHz (1.05–1.45 GHz). At the same time, the reverse isolation ($-S_{12}$) is better than 31 dB over the whole frequency range of the network analyzer (300 kHz–3 GHz). Fig. 8(b) shows that, in the L2 band, the input reflection coefficient (S_{11}) and the output reflection coefficient (S_{22}) are -11 and -11.5 dB, respectively. Both reflection coefficients are better than -10 dB in a 100-MHz-wide band around the GPS L2 frequency of 1.2276 GHz (1.2–1.3 GHz). Due to the increased resistivity of the top metal layer, the $R_{\rm load}$ of the coil became 20% lower than originally simulated, which resulted in a lower S_{21} and a larger S_{22}. The gain degradation has been compensated for by lowering the input impedance to 30 Ω by decreasing the nominal L_s value. The NF of the $50\,\Omega\,R_{\rm S}/30\,\Omega\,R'_{\rm S}$ configuration is approximately the same as in the case of a normal $50\,\Omega\,R_{\rm S}/50\,\Omega\,R'_{\rm S}$ configuration. The NF of the LNA has been measured directly using a noise-figure meter and is plotted in Fig. 8(c). At the GPS L2 frequency, a low NF of 0.8 dB is measured (including the noise of the microstrip lines). In addition, the NF remains below 1.2 dB in the 200-MHz-wide frequency range between 1.1–1.3 GHz. The sensitivity to nearby interferers has also been evaluated. In the L2 band, the IIP3 and the 1-dB compression point are -10.8 and -24 dBm, respectively. It is worth noting that all the measurements have been performed from SMA connector to SMA connector, i.e., without de-embedding the substrate parasitics such as strip-line resistance, connector nonidealities, etc.

The IC has been tested for ESD immunity as well. HBM ESD tests have shown that the LNA is capable of surviving positive ESD pulses up to 0.6 kV (zaps measured with respect to $V_{\rm DD}$) and negative ESD pulses down to -1.4 kV (zaps measured with respect to ground), exceeding the 0.5-kV specification. The bottom diode (D2) protects the input against negative zaps with respect to ground, yielding a protection of -1.4 kV. Positive zaps with respect to $V_{\rm DD}$ are covered by top diode D1. However, the series resistance originally inserted in the $V_{\rm DD}$ path to damp any possible resonance between the power supply bondwire and the decoupling capacitors lies in the discharge path and therefore limits the positive ESD performance to the lower 0.6-kV value. In case of a positive zap with respect to ground, the top protection diode must conduct the positive ESD current to the $V_{\rm DD}$ from where it must be directed to ground through a low-resistance power supply clamp. However, since this clamp was not implemented on the test chip, we could not test the susceptibility to positive ESD pulses with respect to $V_{\rm DD}$. For the same reason, we could only test the susceptibility to negative ESD pulses with respect to ground and not with respect to the $V_{\rm DD}$. Nevertheless, since such a clamp may consist of very large structures which contribute almost no series resistance to the ESD discharge path, the LNA should be able to withstand 0.6-kV positive zaps with respect to ground and -1.4-kV negative zaps with respect to $V_{\rm DD}$. The measurement results are summarized in Table II.

V. Conclusion

This work shows that, even in a standard submicron CMOS technology, an extremely low noise figure (< 1 dB) can be combined with a high gain (20 dB) at the same power consumption as commercially available GaAs LNA solutions. In addition, the IC is fitted with an ESD protection on the RF input, which is capable of protecting the LNA from -1.4 kV to 0.6 kV HBM. This demonstrates that an excellent performance can still be achieved while at the same time providing > 0.5 kV ESD protection.

TABLE II
EXPERIMENTAL RESULTS AT 1.2276 GHz

Supply Voltage	1.5 V
Current consumption	6 mA
Power consumption	9 mW
NF	0.8 dB
S_{21}	20 dB
S_{11}	-11 dB
S_{22}	-11 dB
S_{12}	-31 dB
$IIP3$	-11 dBm
ESD-protection	+0.6 kV / -1.4 kV HBM

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